What is claimed is:

1. A closed air gap interconnect structure comprising:

at least two conductive interconnect lines separated by an air gap, wherein at least one of said lines is connected to at least one conducting via, wherein said lines are supported underneath by a plurality of regions made of a robust support dielectric and capped on top by a cap layer.

2. An interconnect structure according to Claim 1, wherein said conductive interconnect and said conductive via comprise a conductive liner and a conductive fill material.

3. An interconnect structure according to Claim 1, wherein said regions of robust support dielectric form an array of pillars.

4. An interconnect structure according to Claim 1, wherein said regions of robust support dielectric form support beams that lie below said interconnect lines and encases at least one of said conducting via.

5. An interconnect structure according to Claim 1, wherein said regions of robust support dielectric form a support plate that lies below said interconnect lines and encase at least one of said conducting via.

6. An interconnect according to Claim 1, wherein said cap layer is a dielectric barrier comprising a regular array of holes which are closed off with same or different dielectric barrier material.

7. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions

formed by lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric coated on said first sacrificial dielectric and said filled and planarized support regions, said second sacrificial dielectric having lithographically patterned line trenches;

a conductive material filled into said line trenches and said via holes and planarized; and

a stencil with a regular array of holes on said filled line trenches and said second sacrificial dielectric;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and said regular array of holes have been closed off by depositing a cap dielectric thereby forming said closed air gap interconnect structure.

8. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions formed by lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric and an optional hard mask layer disposed on said second sacrificial dielectric; said second sacrificial dielectric and said hard mask having lithographically patterned line trenches;

a conductive material filled into said line trenches and said via holes and planarized such that top of the filled conductive material is substantially coplanar with the top surface of said optional hard mask;

an optional first dielectric cap layer disposed on said hard mask layer; and

a stencil with a regular array of holes on top of said cap layer, wherein said regular array of holes have been transferred into said first cap layer and said hard mask layer by a reactive ion etch process;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and a second dielectric cap has been deposited to pinch off the tops of said regular array of holes in said first cap layer thereby closing off said regular array of holes forming said closed air gap interconnect structure.

9. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions by lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric and an optional hard mask layer disposed on said second sacrificial dielectric coated on said first sacrificial dielectric, said second sacrificial dielectric and said hard mask having lithographically patterned line trenches;

an optional thin conformal dielectric passivation liner layer deposited on said contact via holes and said line trenches;

a conductive material filled into said line trenches and said via holes and planarized such that top of the filled conductive material is substantially coplanar with the top surface of said hard mask;

an optional first dielectric cap layer disposed on said hard mask layer; and

a stencil with a regular array of holes on top of said first cap layer, wherein said regular array of holes have been transferred into said cap layer and said hard mask layer by a reactive ion etch process;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and an optional second dielectric cap has been deposited to pinch off the tops of said regular array of holes in said first cap layer thereby closing off said regular array of holes forming said closed air gap interconnect structure.

10. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions by lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric coated on said first sacrificial dielectric and said filled and planarized support regions, said second sacrificial dielectric having lithographically patterned line trenches;

a conductive material filled into said line trenches and said via holes and planarized;

an optional conductive material cap disposed on top surfaces of said conductive material filled into said trenches; and

a stencil with a regular array of holes on said line trenches and said second sacrificial dielectric and said optional conductive material cap;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and said regular array of holes have been closed off by depositing a cap dielectric thereby forming said closed air gap interconnect structure.

11. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions by

lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric and an optional hard mask layer disposed on said second sacrificial dielectric coated on said first sacrificial dielectric, said second sacrificial dielectric and said hard mask having lithographically patterned line trenches;

a conductive material filled into said line trenches and said via holes and planarized such that top of the filled conductive material is substantially coplanar with the top surface of said hard mask;

an optional conductive material cap disposed on top surfaces of said conductive material filled into said trenches;

an optional first dielectric cap layer disposed on said hard mask layer and said conductive material cap; and

a stencil with a regular array of holes on top of said first dielectric cap layer, wherein said regular array of holes have been transferred into said first dielectric layer and said hard mask layer by a reactive ion etch process;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and a second dielectric cap has been deposited to pinch off the tops of said regular array of holes in said first cap layer thereby closing off said regular array of holes forming said closed air gap interconnect structure.

12. A closed air gap interconnect structure comprising:

a substrate;

a first sacrificial dielectric coated on said substrate, said first coated sacrificial dielectric having therein a patterned set of support regions by lithography and filled and planarized with a robust line support dielectric, said first sacrificial dielectric having therein contact via holes patterned by reactive ion etching;

a second sacrificial dielectric and an optional hard mask layer disposed on said second sacrificial dielectric coated on said first sacrificial dielectric, said second sacrificial dielectric and said hard mask having lithographically patterned line trenches;

a thin conformal dielectric passivation liner layer deposited on said contact via holes and said line trenches;

a conductive material filled into said line trenches and said via holes and planarized such that top of the filled conductive material is substantially coplanar with the top surface of said hard mask; and an optional conductive material cap disposed on top surfaces of said conductive material filled into said trenches;

an optional first dielectric cap layer disposed on said hard mask layer and said conductive material cap; and

a stencil with a regular array of holes disposed on top of said first dielectric cap layer, wherein said regular array of holes have been transferred into said first dielectric layer and said hard mask layer by a reactive ion etch process;

wherein said first and second sacrificial dielectrics have been extracted to form air gaps and a second dielectric cap has been deposited to pinch off the tops of said regular array of holes in said first cap layer thereby closing off said regular array of holes forming said closed air gap interconnect structure.

13. A method of building a closed air gap interconnect structure comprising the steps of:

coating a first sacrificial dielectric on a substrate and patterning a set of support regions therein;

filling and planarizing said support regions with a robust dielectric;

coating a second sacrificial dielectric and an optional hard mask layer;

patterning line trenches and contact via holes in said structure by lithography and reactive ion etching;

depositing an optional thin conformal dielectric passivation liner layer;

filling said line trenches and contact via holes with a conductive liner and conductive fill materials and planarizing them so that top of the fill is substantially coplanar with the top surface of said optional hard mask;

depositing a first dielectric cap layer and forming a stencil with a regular array of holes on top of said cap layer;

transferring said regular array of holes into the cap and the hard mask layers by a reactive ion etch process and extracting said first and second sacrificial dielectrics to form air gaps; and

closing off the air gaps by depositing a second dielectric barrier to pinch off the tops of said regular array of holes in said first cap layer.

14. A method according to Claim 13, wherein said substrate is selected from the group consisting of: a microelectronic chip and a chip carrier.

15. A method according to Claim 13, wherein said first sacrificial dielectric is selected from the group consisting of: organic materials such as poly (methylmethacrylate) (PMMA), poly-para-xylylene, amorphous carbon, poly arylene ethers, polystyrene, polynorbornenes; organosilicate materials such as dense or porous methyl silsesquioxanes, hydrogen silsesquioxanes and mixtures thereof; and amorphous hydrogenated silicon containing chemical vapor deposited films of the general composition comprising Si, C, H, and O.

16. A method according to Claim 13, wherein said support regions are selected from the group consisting of: dielectric pillars and dielectric beams.

17. A method according to Claim 13, wherein said first robust dielectric is a chemically different polymer from said first sacrificial dielectric and is selected from the group consisting of: a polyarylene ether, polyimide, poly-para-xylylene, an organosilicate material, a dense or porous methyl silsesquioxane, hydrogen silsesquioxane, amorphous hydrogenated silicon chemical vapor deposited film of a composition comprising Si, C, H and O, silicon oxide and a mixture thereof.

18. A method according to Claim 13, wherein said second sacrificial dielectric is an organic material selected from the group consisting of: a poly (methylmethacrylate) (PMMA), poly-para-xylylene, amorphous carbon, poly arylene ether, polystyrene, polynorbornene, an organosilicate material, a dense or porous methyl silsesquioxane, hydrogen silsesquioxane, amorphous hydrogenated silicon chemical vapor deposited film of a composition comprising Si, C, H and O and a mixture thereof.

19. A method according to Claim 13, wherein said optional hard mask is selected from the group consisting of: an amorphous hydrogenated film of silicon oxide, silicon nitride, silicon carbide, silicon carbonitride, silicon oxycarbide, tantalum nitride, spin on silsesquioxane glass film and a combination thereof.

20. A method according to Claim 13, wherein said conductive liner is selected from the group consisting of: Ta, W, Ti, conductive nitrides and siliconitrides thereof and a combination thereof.

21. A method according to Claim 13, wherein said conductive fill is selected from the group consisting of: Cu, Ag, Au, Al, W and a combination thereof.

22. A method according to Claim 13 wherein said optional thin conformal dielectric liner layer is selected from the group consisting of: a spin-on film of methyl silsesquioxane or hydrogen silsesquioxane, a CVD deposited film selected from the group consisting of: SiO_2 and amorphous hydrogenated silicon carbide, and a film having a composition comprising Si, C, O, and H.

23. A method according to Claim 13, wherein said dielectric cap layer is selected from the group consisting of: amorphous hydrogenated silicon carbide, nitrided silicon carbide and silicon nitride.

24. A method according to Claim 13, wherein said stencil with holes is formed by an electron, X-ray, EUV, ion or photon lithography, imprint lithography, self-assembly processes, spinoidal decomposition or by phase separation of a polymer blend, a copolymer or a composite.

25. A method according Claim 13, wherein said first and second sacrificial dielectrics is extracted by a method selected from the group consisting of: wet etching, plasma etching, reactive ion etching, thermal means, pyrolysis, supercritical fluid based extraction and a combination thereof.

26. A method according to Claim 13, wherein said second dielectric barrier layer is an amorphous hydrogenated film selected from the group consisting of: silicon oxide, silicon nitride, silicon carbide, silicon carbonitride, silicon oxycarbide and a combination thereof.

27. A method according to Claim 13, wherein the steps therein are repeated at least once to build a multilevel air gap structure.

28. A method of building a closed air gap interconnect structure comprising the steps of:

coating a first sacrificial dielectric on a substrate and patterning a set of support regions therein;

filling and planarizing said support regions with a robust dielectric;

coating a second sacrificial dielectric and a hard mask layer;

patterning line trenches and contact via holes in said structure by lithography and reactive ion etching;

depositing an optional thin conformal dielectric passivation liner layer;

filling said line trenches and contact via holes with a conductive liner and conductive fill materials and planarizing them so that top of the fill is substantially coplanar with the top surface of the hard mask;

forming an optional electrically conductive cap layer on the tops of said conductive fill material features only;

forming a stencil with a regular array of holes on top of said cap layer and said hard mask layer;

transferring said regular array of holes into the hard mask layer by a reactive ion etch process and extracting said first and second sacrificial dielectrics to form air gaps; and

closing off the air gaps by depositing a dielectric barrier to pinch off the tops of said regular array of holes in said hard mask layer.

29. A method according to Claim 28, wherein said optional electrically conductive barrier cap layer is selected from the group consisting of: Ta, TaN, W, WN, Ti, TiN, TiSiN, TaSiN, Co-P, Co-W-P, Co-Sn-P and a combination thereof.

30. A method according to Claim 28, wherein said optional electrically conductive cap layer is formed selectively on the tops of said conductive fill material by a process selected from the group consisting of:

sputtering, evaporation, chemical vapor deposition, atomic layer deposition, electroless plating, electrolytic plating, chemical mechanical polishing, etching and a combination thereof.

31. A method according to Claim 28, wherein the steps therein are repeated at least once to build a multilevel air gap structure.

32. A method of forming an air gap structure comprising the steps of:

coating a robust support dielectric on a substrate and a sacrificial dielectric on said support dielectric;

coating an optional hard mask layer on top of the sacrificial dielectric;

lithographically patterning the optional hard mask and etching line trenches and vias into said sacrificial dielectric and said support dielectric respectively;

lining said line trenches and vias with a conductive barrier;

filling them with a conductive fill material;

planarizing to form interconnect lines and vias such that the top of the fill is substantially coplanar with the top surface of the optional hard mask;

depositing a first dielectric barrier cap layer on top of said interconnect lines and optional hard mask;

forming a stencil with an array of holes on top of said first dielectric cap layer;

transferring the hole pattern into said first dielectric cap and said optional hard mask layers by reactive ion etching; and

extracting said sacrificial dielectric and closing off the hole array by depositing a second dielectric barrier layer to form a closed air gap structure.

33. A method according to Claim 32, wherein the steps therein are repeated at least once to build a multilevel air gap structure.